REMARKS/ARGUMENTS

Claims 6-19 are pending in the present application. Claims 6-8, 11-16, and 18-19 were amended. Reconsideration of the claims is respectfully requested.

I. Examiner Interview

Applicants appreciate the courtesies that were extended by Examiner Lewis Bullock during the interview that was conducted February 21, 2008. Applicants' claims were discussed. No agreement was reached.

II. 35 U.S.C. § 101

The Examiner has rejected claims 11-15 and 18-19 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

With regards to claims 11-15 and 18-19, the examiner states:

> **Claims 11-15 and 18-19** are not limited to tangible embodiments. In view of Applicant's disclosure, specification page 64 in the last paragraph, the medium is not limited to statutory embodiments, instead being defined as including both statutory embodiments (e.g., "recordable-type media, such as a floppy disk") and non-statutory embodiments (e.g., transmission-type media, such as ... radio frequency and light wave transmissions"). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.
>
> Further, claims 11 and 19 recite "A computer program product, which is stored in [and therefore distinct from] a computer readable medium". In view of this language it is reasonable to read the claim as directed to an abstract idea (i.e. a disembodied computer program) who's intended use is to be stored in a computer readable medium and does not itself incorporate the medium. In other words "computer readable instructions stored on a computer readable medium" recite a statutory computer program product (assuming the computer readable medium is also statutory). Whereas, the current claims recite a program product distinct from any physical matter, which is necessary to meet the requirements of 35 USC 101. Claims 10-1 5 and 18 depend from claim 11 and are rejection for the same reasons.

Final Office Action dated October 26, 2007, pages 2-3.

Applicants have amended the specification to cancel the language regarding "transmission-type media." Applicants have also amended claims 11 and 19 to describe the computer program product comprising a computer-readable medium having stored thereon computer-readable instructions. Support for these amendments can be found in the paragraph that starts on page 64, line 15, and ends on page 65, line 3, of Applicants' specification. Therefore, claims 11-15 and 18-19 are limited to tangible embodiments.

III. 35 U.S.C. § 112, First Paragraph

The Examiner has rejected claims 16-19 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed.

The Examiner states:

> Claims 16, and 18-19 recite representing a threshold and count in a second and third "one of the plurality of bits". A single bit is only capable of representing numbers between 0-1. Applicant's disclosure does not enable one of ordinary skill in the art to provide the disclosed and claimed 'threshold' functionality using a count and/or threshold field consisting of a single bit. In other words, a threshold of 1 will be reached each time an instruction is executed. Applicant's specification discloses "Multiple bits may be used to identify a threshold" (see pg. 27, line lo), it is this understanding that will be used in examining the claims. Claim 17 depends from claim 16 and is rejected for the same reason.

Final Office Action dated October 26, 2007, pages 3-4.

Applicants have amended claims 16 and 18-19 to recite: "a second plurality of the plurality of bits identifying the threshold value; a third plurality of the plurality of bits used as a counter to count a number of times each one of the plurality of instructions is executed." Support can be found in the specification on at least page 27, lines 1-15. Therefore, the rejection of claims 16-19 under 35 U.S.C. § 112, first paragraph has been overcome.

IV. 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected claims 11-15 and 18-19 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

As to claims 11-15 and 18-19, the examiner states:

> As noted above, the claims 11 and 19 recite "A computer program product, which is stored in a computer readable medium". This language makes it unclear if applicant is seeking protection for the combination of "computer program product1' and "computer readable medium" or simply the "computer program product" on it's own. Claims 10-1 5 and 18 depend from claim 11 and are rejected for the same reasons.
>
> Claim 11 recites "the caller of a routine" in line 19. There is insufficient antecedent basis for the recitation of "the caller" and it is unclear if the recited "a routine" is intended to refer to the "a routine" introduced in line 13. For the purposes of examination the claim will be treated as reading "a caller of the routine" as recited in claim 6.

Final Office Action dated October 26, 2007, page 4.

Applicants have amended claims 11 and 19 to recite: "the computer program product comprising a computer-readable medium having stored thereon computer-readable instructions."

Applicants have amended claim 11 to correct the antecedent basis.

Therefore the rejection of claims 11-15 and 18-19 under 35 U.S.C. § 112, second paragraph has been overcome.

V. 35 U.S.C. § 103, Obviousness

V.A. *Lueh* in view of *Partamian* in view of *Buser*

The examiner has rejected claims 6-18 under 35 U.S.C. § 103 as being unpatentable over *Lueh* (U.S. Patent Number 6,966,057)(hereinafter "*Lueh*") in view of *Partamian et al.* (U.S. Publication Number 2003/0225917)(hereinafter "*Partamian*") in view of Buser (U.S. Publication Number 2004/0030870)(hereinafter "*Buser*"). This rejection is respectfully traversed.

Applicants have amended the independent claims to describe similar features. Claim 6 is representative of the other independent claims. Claim 6 recites, in part:

> an instruction cache, which is included in a processor, that outputs said plurality of instructions to a sequencer unit that outputs the plurality of instructions to execution units for executing the plurality of instructions, wherein the sequencer unit and execution units are included in the processor;
>
> the instruction cache for using said indicator to detect execution of each one of the plurality of instructions, wherein execution of instructions, which are not associated with the indicator, is not detected;
>
> the instruction cache sending a signal to a performance monitor unit responsive to the instruction cache detecting said indicator in a particular one of the plurality of instructions, wherein the particular one of the plurality of instructions is located in a routine, and further wherein the signal is not sent to the performance monitor unit for instructions that are not associated with the indicator, and further wherein the signal indicates that the particular one of the plurality of instructions is being executed, and still further wherein the performance monitor unit is coupled to each functional unit of said processor;
>
> the performance monitor unit counting events that are associated with an execution of only said plurality of instructions that are associated with the indicator responsive to the performance monitor unit receiving the signal;
>
> collecting means for collecting data from the performance monitor unit;
>
> using means for using said data to identify a caller of the routine;

The combination of *Lueh*, *Partamian*, and *Buser* does not render Applicants' claims obvious because the combination does not teach or suggest these features.

Lueh teaches a platform debugger architecture 145. The platform debugger architecture 145 includes a debuggee 210, which is a process that is being debugged. Debuggee 210 includes an

application 212 that is being debugged. The application 212 includes a compilation infrastructure 310 and debugging support 370. The debugging support 370 includes control break-point support 430 and data break-point support 440. *Lueh* teaches break-points being implemented using trap patching and code patching. A location map is provided where the original code needs to be replaced with a branch or trap instruction.

The Examiner asserts, on page 5, paragraph 13, that *Lueh* teaches:

> an instruction cache, which is included in a processor, for using said indicator to detect execution of each one of the plurality of instructions, wherein execution of instructions, which are not associated with the indicator, is not detected (col. 6, lines 1-3 "original code needs to be replaced with a branch or trap instruction," col. 5, lines 57-67 "Breakpoints can be implemented using ... trap patching and code patching" note that instructions not indicated in the "location map" will not be monitored and thus their execution will not be detected)."

Final Office Action, mailed October 26, 2007, page 5.

The Examiner does not, however, specifically indicate what element in *Lueh* the Examiner believes is analogous to an instruction cache that performs this step.

Lueh does not teach an instruction cache, which is included in a processor, that outputs said plurality of instructions to a sequencer unit that outputs the plurality of instructions to execution units for executing the plurality of instructions, wherein the sequencer unit and execution units are included in the processor. *Lueh* teaches a processor 110, but does not teach the processor including an instruction cache, sequencer unit, and execution units where the instruction cache outputs said plurality of instructions to a sequencer unit that outputs the plurality of instructions to execution units for executing the plurality of instructions.

The Examiner asserts that *Lueh* teaches an indicator by teaching a location map, where the original code needs to be replaced with a branch or trap instruction. The Examiner asserts that *Buser* teaches breakpointing in which an indicator is stored in at least one existing spare bit in each one of a plurality of instructions. The Examiner asserts that *Buser* provides an alternate means of providing breakpoints.

Applicants claim the instruction cache sending a signal to a performance monitor unit responsive to the instruction cache detecting said indicator in a particular one of the plurality of instructions, wherein the particular one of the plurality of instructions is located in a routine, and further wherein the signal is not sent to the performance monitor unit for instructions that are not associated with the indicator, and further wherein the signal indicates that the particular one of the plurality of instructions is being executed, and still further wherein the performance monitor unit is coupled to each functional unit of said processor. Applicants also claim the performance monitor unit counting events that are associated with execution of only said plurality of instructions that are associated with the indicator responsive to the

performance monitor unit receiving the signal. The combination of *Lueh*, *Partamian*, and *Buser* does not render Applicants' claims obvious because the combination does not teach or suggest these features.

The combination of *Lueh*, *Partamian*, and *Buser* does not teach an instruction cache sending a signal to a performance monitor unit responsive to the instruction cache detecting the indicator in a particular instruction. The combination does not teach sending a signal to a performance monitor unit upon a branch or trap instruction, where the performance monitor unit counts events that are associated with the execution of the plurality of instructions.

Applicants claim collecting data from the performance monitor unit; and using said data to identify a caller of the routine. The Examiner asserts that *Lueh* teaches the monitoring program identifying information regarding a caller of the routine. Specifically, the Examiner states that the JIT compiler provides a mechanism to identify and access the caller's frame context, referred to as unwinding the stack frame. Unwinding the stack frame to identify a caller's frame context does not teach using data, which was collected from a performance monitor unit, to identify a caller of the routine.

Claims 7-10 and 16-17 depend from claim 6 and are patentable for the reasons given above with regard to claim 6. Claims 12-15 and 18 depend from claim 11, which recites features that are similar to the features recited by claim 6; therefore, claims 12-15 and 18 are patentable for the reasons given above.

Therefore, the rejection of claims 6-18 under 35 U.S.C. § 103 has been overcome.

V.B. *Lueh* in view of *Blandy* in view of *Buser*

The Examiner has rejected claim 19 under 35 U.S.C. § 103 as being unpatentable over *Lueh* in view of *Blandy et al.* (U.S. Patent Number 5,896,538)(hereinafter "*Blandy*") in view of *Buser*. This rejection is respectfully traversed.

The Examiner states:

> **Regarding Claim 19:** Claim 19 primarily recites a combination of the limitations addressed separately in claims 6-10 and 16-17.
>
> Blandy teaches a threshold value used to identify a hot method (col. 3, lines identifies the hot modules ... After a module has been called a certain number of times") similar to, and resulting in the same obvious modifications as the Partamian teaching relied upon in the rejection of claims 6-10 and 16-17.
>
> Further, Blandy teaches a "performance monitor may track the cycle time for a module" (col. 3, lines 8-10). Accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to use cycle time for the threshold value as an alternative means of determining a hot method.

Final Office Action dated October 26, 2007, pages 10-11.

Blandy teaches keeping track of the number of times a module is executed by counting CALL and RETURN instructions. *Blandy* also teaches tracking the cycle time for a module.

The combination of *Lueh*, *Blandy*, and *Buser* does not render Applicants' claim 19 obvious for the reasons given above regarding the combination of *Lueh* and *Buser*, and because *Blandy* does not cure the deficiencies of the combination of *Lueh* and *Buser*. Therefore, the rejection of claim 19 under 35 U.S.C. § 103 has been overcome.

VI. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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